Changes to the Claims

Claims 1-40 (cancelled)

41. (Original) An emitter, comprising:

an emitting surface having a first area;

a first chamber having substantially parallel sidewalls interfacing to the emitting surface; and

a second chamber interfacing to the first chamber and having sidewalls diverging to an opening having a second area larger than the first area.

42. (Original) The emitter of claim 41, further comprising a cathode layer disposed on the emitting surface, and sidewalls of the first and second chambers and wherein the emitter has been subjected to an annealing process thereby increasing the emission capability of the emitter.

43. (Original) The emitter of claim 41 wherein the first chamber is formed within an adhesion layer.

44. (Original) The emitter of claim 41 wherein the second chamber is formed within a conductive layer.

45. (Original) An integrated circuit comprising at least one emitter of claim 41.

46. (Original) A display device comprising at least one emitter of claim 41.

47. (Original) A storage device comprising at least one emitter of claim 41.

48. (Original) An integrated circuit, comprising:

a conductive surface to provide an electron supply;

at least one emitter formed on the electron supply including,

an insulator layer having at least one opening to define the location and shape of the at least one flat emitter device,

a conductive layer disposed over the insulator layer, the conductive layer having at least one opening in alignment with the at least one opening;

a tunneling layer disposed within the at least one opening of the insulator layer; and

a cathode layer disposed over the tunneling layer and partially over the conductive layer.

49. (Original) The integrated circuit of claim 48 wherein the tunneling layer is a metal cluster dielectric.

50. (Orignal) The integrated circuit of claim 48 wherein the tunneling layer has a thickness less than about 500 Angstroms.

51. (Original) The integrated circuit of claim 48 wherein the tunneling layer has a thickness between about 50 Angstroms and about 250 Angstroms.

52. (Original) The integrated circuit of claim 48 wherein the tunneling layer is TiO_x.

53. (Original) The integrated circuit of claim 48 wherein the tunneling layer is a metal cluster dielectric selected from the group consisting of TaO_x, WSiN, TaO_xN_y, $TaAlO_xN_y$, $TaAlO_x$, and AlO_xN_y.

54. (Original) The integrated circuit of claim 48 wherein the integrated circuit has been subjected to an annealing process.

Claims 55-71 (Cancelled).